Application Note 221
DS276x Product Comparison

Introduction

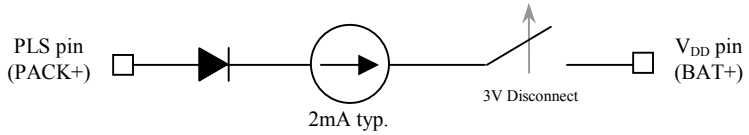
The DS2762, DS2761, and DS2760 die revision C2 provide upgrades to the operation of the original DS2760 (die revisions B2 and B3). The differences between these devices are minor and can cause confusion as to whether or not system hardware and software updates are needed to transition use from one to another. Table 1 summarizes the functional differences between all DS276x devices.

Table 1. Summary of Device Differences

FEATURE	DS2760B2/B3	DS2760C2	D2761	DS2762
Low-Voltage Recovery		✓	✓	✓
$\overline{PS}$ Latch			✓	✓
PLS Pulldown			✓	✓
Charge FET Enable During Discharge			✓	✓
$\overline{PS}$ & DQ Delays				✓
Threshold Alarms				✓
Increased ESD Immunity				✓

Low-Voltage Recovery Operation

The DS2760C2, DS2761, and DS2762 provide a maximum 10mA (2mA typical) charge path from the PLS pin to the V_{DD} pin. A depleted cell can be charged through this path to a point sufficient to power the chip and allow normal charge. This path operates in parallel with any external charge path and otherwise does not affect normal operation of the IC. The cell cannot be discharged through the recovery path by pulling PLS low. Low-voltage recovery is disabled above 3.0V to prevent cell overcharge.

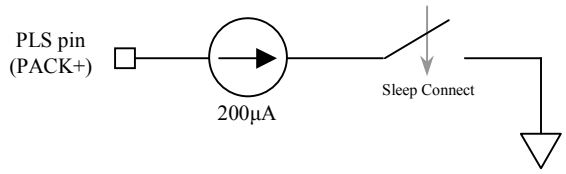


$\overline{PS}$ Bit Latch Operation

The DS2761 and DS2762 latch the low state of the $\overline{PS}$ bit (bit 7 of the special feature register). This bit is not latched on the DS2760 and will return to high with the $\overline{PS}$ pin. Existing application software or test code that accesses the $\overline{PS}$ bit should be modified to write this bit to a 1 to clear the latch after a 0 is read. If the existing system does not access the $\overline{PS}$ bit, no changes are necessary. Operation of the $\overline{PS}$ pin and device sleep mode are unaffected by this change.

PLS Pulldown Operation

The DS2761 and DS2762 provide a 200µA pulldown on the PLS pin while in sleep mode. This new feature is only present while the chip is in sleep mode and prevents PACK+ from floating and possibly generating a false charger detection by the IC. It does not require any system or software changes if upgrading from the DS2760.



Charge FET Enable during Discharge

When an Overcharge condition occurs, the charge FET is disabled to prevent further charging of the cell. The DS2760 requires the cell voltage to drop below the charge enable threshold (V_{CE}) before re-enabling the charge FET. The DS2761 and DS2762 immediately re-enable the charge FET if a discharge current greater than 80mA is detected on internal resistor devices or $V_{IS1} - V_{IS2} > 2mV$ on external resistor devices. This prevents power loss and heat generation through the body diode of the charge FET. This function occurs automatically and does not require any system or software changes if converting from the DS2760 to the DS2761 or DS2762.

$\overline{PS}$ and DQ Pin Delays

The DS2762 incorporates 100ms delays on the rising edge of DQ and the falling edge of $\overline{PS}$ before entering the active mode of operation. This prevents glitches on these lines from causing the device to accidentally exit sleep mode. Normal operation of the DQ line is unaffected by this change. This function occurs automatically and does not require any system or software changes if converting from the DS2760 or DS2761 to the DS2762.

Threshold Alarms

The DS2762 features an Alarm function that generates an interrupt on the PIO line if the temperature or accumulated current readings exceed preset limits. This feature is enabled by setting IE, bit 2 of the status register, to a '1'. User RAM locations 0x80 through 0x85 are then used to set upper and lower limits to compare the ACR and temperature registers to. Normal PIO operation is disabled during this time.

Increased ESD Immunity

The DS2762 also offers increased ESD protection against corruption of user RAM locations as well as the real time registers and the event flags. The internal Power on Reset circuitry has also been adjusted to prevent ESD from causing a device reset. The recommended applications circuit in the datasheet should provide sufficient ESD protection for most applications.

Summary

There is essentially very little functional difference between different die revisions of the DS276x. The DS2761 and DS2762 operate identical to the DS2760 with the addition of several feature enhancements. The $\overline{PS}$ bit latch can require a small software change for compatibility. All other enhancements function automatically and the DS2761 or DS2762 will drop into a DS2760-based application with no system hardware changes.